

WHAT IS CLAIMED IS:

1           1.     An integrated circuit comprising:  
2           a graphics pipeline; and  
3           a frame buffer interface,  
4           wherein the graphics pipeline comprises a shader coupled to a texture cache, the  
5   shader further coupled to the frame buffer interface,  
6           wherein the shader stores and loads data to and from an external graphics memory  
7   using the frame buffer interface, and the shader is configured to store and load data to and from  
8   specific locations in the external graphics memory during a single pass through the graphics  
9   pipeline.

1           2.     The integrated circuit of claim 1 wherein the shader executes instructions  
2   forming a shader program, the shader program executed during a plurality of passes.

1           3.     The integrated circuit of claim 2 wherein one of the plurality of passes  
2   comprises:  
3           executing a first plurality of instructions;  
4           executing a read command, wherein data is read from a buffer in the external  
5   graphics memory and received by the shader using the frame buffer interface; and  
6           executing a second plurality of instructions.

1           4.     The integrated circuit of claim 2 wherein one of the plurality of passes  
2   comprises:  
3           executing a first plurality of instructions;  
4           executing a write command, wherein data is written to a buffer in the external  
5   graphics memory by the shader using the frame buffer interface; and  
6           executing a second plurality of instructions.

1           5.     The integrated circuit of claim 1 wherein the shader may write to and read  
2   from a first number of buffers located in the external graphics memory, the first number greater  
3   than two.

- 1                   6.     The integrated circuit of claim 3 wherein the first number of buffers are  
2 read-only buffers.
- 1                   7.     The integrated circuit of claim 5 wherein the first number of buffers are  
2 read/write buffers.
- 1                   8.     A method of generating a computer graphics image comprising:  
2                   executing a first plurality of instructions in a shader program, the shader program  
3 running in a shader in a graphics pipeline, the shader program executed during a plurality of  
4 passes through the shader;  
5                   executing a load command, wherein data is read from a first buffer by the shader;  
6 and  
7                   executing a second plurality of instructions in the shader program,  
8                   wherein the first plurality of instructions, the load command, and the second  
9 plurality of instructions are executed during a single pass through the shader.
- 1                   9.     The method of claim 8 wherein the shader may load data from a plurality  
2 of buffers, the plurality of buffers exceeding two buffers.
- 1                   10.    The method of claim 8 further comprising:  
2                   executing a store command, wherein data is stored by the shader in a second  
3 buffer; and  
4                   executing a third plurality of instructions in the shader program,  
5                   wherein the first plurality of instructions, the load command, the second plurality  
6 of instructions, the store command, and the third plurality of instructions are executed during a  
7 single pass through the shader.
- 1                   11.    The method of claim 10 wherein the shader may store data in and load  
2 data from a plurality of buffers, the plurality of buffers exceeding two buffers.
- 1                   12.    The method of claim 11 wherein the buffers are located in an external  
2 graphics memory.

1                   13.    The method of claim 12 wherein the shader stores data in and loads data  
2   from the buffers using a frame buffer interface.

1                   14.    An integrated circuit comprising:  
2                   a frame buffer interface; and  
3                   a graphics pipeline coupled to the frame buffer interface, the graphics pipeline  
4   comprising a shader coupled to a texture cache,  
5                   wherein the shader may access a plurality of buffer storage locations in a graphics  
6   memory using the frame buffer interface,  
7                   wherein the plurality of buffer storage locations exceeds two storage locations.

1                   15.    The integrated circuit of claim 14 wherein the graphics memory is not on  
2   the integrated circuit.

1                   16.    The integrated circuit of claim 15 wherein the shader may read data from  
2   the plurality of storage locations using the frame buffer interface.

1                   17.    The integrated circuit of claim 15 wherein the shader may read data from  
2   and write data to the plurality of storage locations using the frame buffer interface.

1                   18.    The integrated circuit of claim 17 wherein the shader reads and writes data  
2   to and from the plurality of storage locations using the frame buffer interface by using load and  
3   store commands in the shader program that include storage location identifications.

1                   19.    The integrated circuit of claim 17 wherein the shader reads and writes data  
2   to and from the plurality of storage locations using the frame buffer interface by using load and  
3   store commands in the shader program that include a direct reference to storage location  
4   addresses in the graphics memory.

1                   20.    The integrated circuit of claim 17 wherein the shader reads and writes data  
2   to and from the plurality of storage locations using the frame buffer interface by using load and  
3   store commands in the shader program that include indirect references to storage location  
4   addresses in the graphics memory.